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(54) Method and apparatus for the production of a semiconductor

(57) A semiconductor substrate is, during surface treatment such as ion implantation, surrounded by or supported by a frame, vessel, jig or container, which has a thin coating of material, eg a semiconductor, compatible with the semiconductor substrate, or having no undesirable influence thereon, so as to avoid or reduce deposition of unwanted impurities on the semiconductor surface. Preferably the coating has substantially the same coefficient of thermal expansion as the base material of the container, but if not then an intermediate layer may be provided between the coating and the base material.

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SPECIFICATION

Method and apparatus for the production of semiconductors

This invention relates to the production of semiconductors and more particularly it is concerned with the avoidance or reduction of the deposition of unwanted impurities on the surface of a semiconductor during surface treatment or doping thereof.

In the production of a semiconductor, it is usual to introduce selected impurities, such as donors or acceptors, and for this purpose it is usual to employ either of two methods, namely thermal diffusion and ion implantation. Of these two, ion implantation has generally been thought preferable for the incorporation of impurities to a required depth and to a required concentration. The present invention is particularly concerned with ion implantation but is not restricted to it.

Ion implantation is ordinarily performed by disposing a semiconductor substrate, which is usually earthed, in an evacuated vessel and applying, by means well-known in themselves, ions with an energy between several tens of kilo-electron-volts to several mega-electron-volts. When such ion implantation is performed, it is usual to provide a jig or other support means to hold the semiconductor substrate. The support means may be made of a ferrous metal, a ferrous alloy such as stainless steel, an aluminium alloy or a titanium alloy. During ion implantation, it is usual to scan the semiconductor substrate by means of the ion beam in order to implant the ions in a controlled manner. However, the ion beam almost inevitably impinges not only on the substrate but also the jig or other support means and the inner wall of the vacuum vessel. The result is usually a sputtering phenomenon and it is common to find that unwanted impurities such as iron, titanium and aluminium adhere to the surface of the semiconductor substrate. The adhesion of these impurities results in various undesirable effects, such as an increase in conductivity of a region which should be, for example, intrinsic or insulative other undesirable effects such as the creation of barrier layers or the undesirable alteration of lattice parameters and such like. The resultant components may exhibit various faults, such as a reduction in speed of operation. It will be understood that the undesirability of the impurity depends on the particular process.

It is the general object of the present invention to improve the production of semiconductors and in particular to avoid or reduce the contamination of a semiconductor during surface treatment or the doping or implantation of the semiconductor with desired impurities.

Broadly stated, the present invention is characterised in that the parts (i.e. jig or other support and/or the vacuum vessel) surrounding or supporting the semiconductor substrate which is subjected to treatment is partly or completely coated with a material which is compatible with the desired characteristics of the treated substrate, i.e., has no unfavourable effect upon the semiconductor substrate. Thus if there is, for example, sputtering from the surrounding parts, the coating material may be deposited on the surface of the semiconductor but will not substantially affect the treated semiconductor.

The surface treatment of the said parts to provide said coating may be carried out by ion implantation, chemical vapour deposition, plasma chemical vapour deposition, sputtering or ion plating.

The material employed for the coating may be the same as or similar to the material of the semiconductor which is to be treated. By "similar to" is meant in general a material having similar lattice parameters or a semiconductor of the same conductivity type though having possibly different doping levels. If silicon is employed as the material for the semiconductor substrate, the prior coating of the surrounding or supporting parts may be of silicon or Group III-V compounds such as gallium arsenide and indium phosphide or Group II-VI compound semiconductors such as zinc sulphide or zinc selenide. Alternatively, if the semiconductor substrate is a Group III-V compound, the coating may be another Group III-V compound or silicon. Likewise, if the semiconductor substrate is zinc sulphide or zinc selenide, it may be possible to employ either silicon or gallium arsenide or indium phosphide as the material for coating the surrounding parts.

As a base material of the surrounding parts, there may be employed a ferrous alloy, an aluminium alloy, a titanium alloy or a suitable ceramic material. In any event it is preferable to select a base material of which the coefficient of thermal expansion is not substantially different from that of the coating material. If the coefficients of thermal expansion of the base material and the coating material are substantially different, an intermediate layer or layers may be inserted between the base material and the coating layer.

The said surrounding parts may be a jig for holding the semiconductor substrate, the vacuum vessel and surrounding parts such as heaters, electrodes, transport mechanisms and such like and the advantages or effects of the present invention may be obtained by coating the whole or some of the surface of the surrounding parts.

Examples

EXAMPLE 1

A silicon wafer was held by parts consisting of a base material of stainless steel (SUS 304) coated with a silicon layer of 5 micrometres in thickness by sputtering. The silicon wafer was subjected to doping with boron by ion implantation employing an accelerating voltage of 100 kilo-electron-volts and a dosage of $5 \times 10^{13}/cm^2$ to obtain Sample 1.

For comparison, the same silicon wafer was subjected to the same boron-doping treatment without any coating of the stainless steel to obtain Comparative Sample 1.

The surfaces of the resulting samples were subject to spectral analysis using Auger electron spectroscopy. No detectable contamination was found on the surface of Sample 1 but the surface of Comparative Sample No. 1 exhibited 2.3% iron, 0.5% chromium and 0.2% nickel.

EXAMPLE 2

A gallium arsenide wafer was held by a support consisting of a base material of an aluminium-copper

alloy coated with a gallium arsenide layer of 10 micrometres in thickness by a metal oxide chemical vapour deposition method and then subjected to doping by aluminium by ion implantation with an accelerating voltage of 200 kilo-electron-volts and a dose of $7 \times 10^{14}/cm^2$ to obtain Sample No. 2.

For comparison, the same gallium arsenide wafer was subjected to the same doping treatment without any coating of the aluminium-copper alloy to obtain Comparative Sample No. 2.

When memory elements were prepared from these samples by similar processes, the yields were 92% in the case of Sample 2 and 65% for Comparative Sample No. 2.

EXAMPLE 3

A silicon wafer was held by parts consisting of a base material of a titanium-aluminium-vanadium alloy coated with an intermediate layer of titanium nitride of 3 micrometres in thickness by an ion plating method and then with an indium phosphide layer of 1 micrometres in thickness by an MBE method and then subjected to phosphorus-doping by an ion implantation method with an accelerating voltage of 80 kilo-electron-volts and a dose of $4 \times 10^{13}/cm^2$ to obtain Sample 3.

For comparison the same silicon wafer was subjected to the same phosphorus-doping treatment without coating of the titanium-aluminium-vanadium alloy of the parts to obtain Comparative Sample No. 3.

When memory elements were prepared from these samples by a similar process, the memory elements obtained from Sample No. 3 showed an increase of 50% in reading and writing speeds over that of Comparative Sample No. 3.

CLAIMS

1. An apparatus for the production of a semiconductor, the apparatus comprising a jig or other support or container for a semiconductor substrate while the substrate is subjected to a surface treatment, at least part of the support or container being coated with a material having no undesirable influence upon the semiconductor substrate.

2. Apparatus according to claim 1 wherein the coating comprises a semiconductor material.

3. Apparatus according to claim 2 wherein the semiconductor substrate comprises silicon and the coating material comprises either silicon or a Group III-V semiconductor or a Group II-VI semiconductor.

4. Apparatus according to any foregoing claim wherein the said support or container is made of iron or aluminium, or titanium or alloys thereof.

5. Apparatus according to any foregoing claim wherein the coating material has substantially the same coefficient of thermal expansion as the base material of the said support or container.

6. Apparatus according to claim 1 wherein the coating material has a coefficient of expansion different from that of the base material and an intermediate layer is provided between the two.

7. A method for the production of semiconductor devices comprising subjecting a semiconductor substrate to ion implantation, the semiconductor substrate being surrounded or supported by parts primarily composed of a base material which if sputt red on to the surface of the semiconductor substrate by virtue of impingement of a beam of ions thereto adversely affects the quality or performance of said devices, a substantial proportion of the surface of the said being previously coated with a material which is compatible with the semiconductor substrate as implanted.

8. A method according to claim 7, wherein the semiconductor comprises silicon and the coating comprises either silicon or a Group III-V semiconductor compound, or a Group II-VI semiconductor compound.

9. A method according to claim 7 wherein the semiconductor and the coating comprise gallium arsenide.

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